2.4 Deep Trench Isolation of IC Transistors

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Introduction

At present many modern bipolar processes are exploiting trench isolation to improve electrical characteristics [1]. Deep trench isolation offers great advantages over more conventional junction isolation of adjacent IC transistors. Improved packing densities can be achieved and the parasitic sidewall capasitance associated with the junction isolation is totally eliminated. By using this isolation approach it is possible to utilize epitaxially grown buried layer in bipolar transistors. The damage caused by buried layer implantation is eliminated and the collector material is of higher crystalline quality. The main requirements for the trenches are vertical walls and voidless and seamless refill. These undesirable voids and the seam in the centre of the filling material may cause generation of defects during subsequent heat treatments and oxidation. In this study, a fabrication method for polysilicon filled trenches has been depicted.

Experimental

The test sample preparation was started with growth and lithography of low-pressure chemical vapour deposited (LPCVD) TEOS (tetraethoxy silane) oxide to mask the test pattern for deep silicon etching. Deep silicon etching was accomplished in inductively coupled plasma (ICP) etcher (STS Multiplex) using fluorine-based chemistry process, so called Bosch process, which propagates using the concept of sequentially switching between etch (SF_6) and passivation (C_4F_8). The duration of etching and passivation steps were both 5 seconds. The etching was accomplished at the RF power of 600W with biasing of 8W. In passivation pulse the bias was lower, only 2W. The total etch time was 5 minutes and the etch depth was 5 µm. After the ICP etching procedure the masking oxide was removed by wet etching in buffered HF. The refill process consisted of first lining the trenches with oxide. This was carried out by oxidizing the test samples in dry O_2 at 850°C for 55 minutes resulting in 35nm thick (liner) oxide. 800nm undoped LPCVD polysilicon was deposited at 625°C on top of the liner oxide to fill the trenches. The planarization was accomplished by etching back the polysilicon in Cl_2/He plasma with slight over etch of 10% in a Lam 590 reactor. The thin liner oxide was used as an etch-stop for planarization etch and prevented the etching of underlying silicon.

Results

The switching approach of ICP etching normally induces the formation of scallops on the sidewalls of the trenches. Switching induced scallops can be observed in Fig. 1a, where the cross-section of a 1.1 µm trench is characterized using scanning electron microscope. The size of such scallops should be minimized to attain voidless filling with polysilicon. Besides that the liner oxide has been used to reduce the surface states on silicon-polysilicon interface thus improving the isolation, it has also been used to smoothen the sidewalls of the trenches. 0.65 µm and 1.1 µm wide, 5µm deep trenches filled with polysilicon is depicted in Fig. 1b. There is no voids at the bottom of the trench visible in the figure and the seam in the polysilicon down the centre of the trench is not observed. These both indicate excellent step coverage of our LPCVD polysilicon.

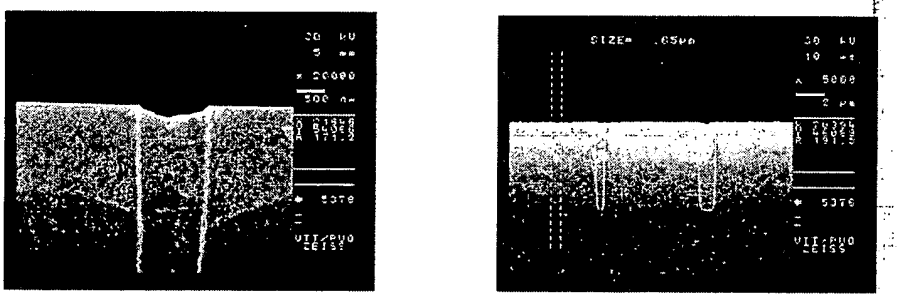

Figure 1. a) A profile of ICP etched trench, filled with polysilicon and planarized, showing small scallops on sidewalls. b) 0.65 and 1.1 µm wide trenches after liner oxidation and LPCVD polysilicon filling. Uniform etch depth can be observed between the narrow and wide trenches.

every few seconds back and forth between etching and polymerizing chemistries. The Bosch process is commonly used to produce high rate anisotropic trench etching of silicon. During the etch chemistry step, rapid isotropic etching of the silicon occurs. During the polymerizing chemistry portion of the process all exposed surfaces of the substrate are coated with polymer. During the next etch chemistry portion of the process, ion bombardment removes the polymer from the bottom of the trench normal to the direction of ion motion, and a isotropically etched cavity is then created. The Bosch process results in microscopic "scallops" on the trench sidewalls being etched. The degree of sidewall scalloping may be controlled by varying the length of each etch - polymer deposition cycle. See also, inductively coupled plasma.

Boule - in order to grow wafers, a large ingot is drawn from a molten silicon melt. The ingot is also referred to as a boule.

Breakdown - when a critical field is exceeded in an insulator or semiconductor, the material breaks-down electrically allowing current to flow.

Breakdown Voltage - the voltage at which breakdown occurs.

BTAB - see Bumped Tape Automated Bonding

Bubbler - a Pyrex glass or quartz container with an inlet tube that extends down to near the bottom of the vessel and an outlet tube located near the top of the vessel. When filled with liquid, a gas may be introduced throng the inlet tube and the gas will bubble through the liquid and exit through the outlet tube. Bubblers are used to introduce vapor from a liquid source into a gas.

Buffered Oxide Etch - an etching solution containing hydrofluoric acid, HF, and ammonium fluoride, NH_3F. The hydrofluoric acid etches silicon dioxide and the ammonium fluoride raises the solution pH reducing the attack rate of the solution on photoresist.

Bumped Die - die that have had tiny solder or gold bumps formed on the bond pads.

Bumped Tape Automated Bonding - a process where bumped die are attached to metal leads mounted on a tape carrier. See also, tape automated bonding.

Bumping - the process of forming solder or gold bumps on bond pads of a die. The bumps may be formed by electroplating or evaporation.

Burn-In - the use of elevated temperature and or electrical stress to cause infant mortality failures so they may be removed prior to shipping product to a customer. Burn-In is common on new products until yield enhancement efforts have increased yield and decreased defect density.

Buried Layer - a low resistivity - doped layer underneath the surface of a semiconductor. Buried layers may be formed by pre deposition - diffusion followed by epitaxial growth, ion implantation and diffusion followed by epitaxial growth or by high energy ion implantation.

Butyl Acetate - chemical formula $CH_3COO(CH_2)_3CH_3$, butyl acetate is a flammable solvent used primarily as a negative photoresist post develop rinse. Butyl acetate is commonly sold as a 100% solution and has a density of 0.88Kg/L. Skin contact and breathing of butyl acetate vapor should be avoided.

Byte - a unit of computer memory, typically 8 bits in length. The smallest addressable unit of memory and most commonly represents a single character such as a letter.

Back to Top